UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/521,852	03/09/2000	Kiyoji Hane	Q58163	2975

7590 12/19/2003

Sughrue Mion Zinn Macpeak & Seas PLLC
2100 Pennsylvania Avenue N W
Washington, DC 20037-3202

EXAMINER	
REITZ, KARL	

ART UNIT	PAPER NUMBER
2624	9

DATE MAILED: 12/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/521,852	HANE ET AL.	
	Examiner	Art Unit	
	Karl R. Reitz	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/17/2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Okazawa (5,937,148).

3. In accordance with claim 1, Okazawa discloses an electronic printing apparatus 100-1 (figure 1), which receives and prints image data; in Okazawa's system, the controller section of the apparatus receives printing data and the engine section of the apparatus prints the image data (col. 4 lines 9-16).

4. Okazawa further discloses that the apparatus contains a print controller 110 (figure 1) for receiving image data (col. 4 lines 9-10) and controlling print sequence; in Okazawa's system, the controller section 110 has a program for controlling the entire apparatus (col. 4 lines 33-34). Okazawa further discloses that the controller contains image memory for storing image data (col. 4 lines 26-27).

5. Okazawa further discloses that the apparatus contains a print engine 120 (figure 1 and col. 4 lines 6-8). Okazawa further discloses that the printing engine prints images on a printing medium in accordance with a signal corresponding to the image data supplied by the print controller (col. 4 lines 58-61).

6. Okazawa further discloses that the print controller is able to operate in a normal operating mode and an energy saving mode, which uses less energy than the normal mode; in Okazawa's system an interface processor 111 (figure 1) controls power to the controller and the engine, and is able to limit power supplied to the controller and the engine in a sleep state (col. 4 line 67 – col. 5 line 6). Thus Okazawa meets all the limitations of claim 1.

7. Claim 2 is rejected under 35 U.S.C. 102(e) as being unpatentable over Okazawa.

8. In accordance with claim 2, Okazawa further discloses that in the normal mode, the print controller stores image data in an image memory (col. 4 lines 26-27). Okazawa further discloses that in the energy saving mode, the print controller stores a recovery program used to return to normal mode in the RAM 116 (figure 1); in Okazawa's system, only the interface processor 111 and the RAM 116 receive power during the sleep mode (col. 7 lines 36-39), thus during sleep mode, control processing is performed by the interface processor 111 (col. 7 lines 40-41) through the use of information stored in RAM 116 (col. 7 lines 1-4). The RAM 116 would also be usable as image memory, as image memory is RAM (disclosure page 7 lines 8-10).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of JP 64-20185.

11. In accordance with claim 3, Okazawa further discloses that the print controller 110 (figure 1) contains a CPU 114 for executing required programs (col. 6 lines 57-60).

12. Okazawa further discloses an interface circuit 150 for receiving image data and interrupts; in Okazawa's system the interface section 150 receives image data from hosts 130-1 or 130-2 and upon receipt of image data, an interrupt signal is generated from the interface processor 111 in the interface section 150 (col. 4 lines 54-58 and col. 7 lines 4-6).

13. Okazawa further discloses a program memory (ROM 115), in which programs for controlling printing and recovery are stored (col. 5 lines 59-61).

14. Okazawa further discloses a band memory (image memory) in which image data to be printed are stored (col. 4 lines 26-27).

15. Okazawa further discloses a control circuit, in the form of the RAM 116, which is connected to the CPU, the interface circuit, and the program memory, via bus 118 (figure 1). Further, the RAM 116 would also be usable as image memory, as image memory is RAM (disclosure page 7 lines 8-10).

16. Okazawa does not disclose expressly that when shifting to energy saving mode, a recovery program is loaded from program memory to image memory.

17. JP 64-20185 discloses that when transferring to energy saving mode, the CPU transfers a program stored in the ROM to the RAM (page 1 line 26 – page 2 line 3).

18. Okazawa and JP 64-20185 are combinable because they are from the same field of endeavor, namely energy saving image forming apparatuses.

19. Therefore, it would have been obvious to a person of ordinary skill in the art to transfer a recovery program from the ROM 115 of Okazawa's system to the RAM 116 when entering energy saving mode, since in Okazawa's system the RAM 116 and the interface processor 111 are the only components which receive energy during energy saving mode (col. 7 lines 36-38).

20. The motivation for doing so would have been to operate only the RAM 116 and the interface processor 111 in the energy saving mode, thus reducing power consumption as compared with maintain power to other portions of the controller section (Okazawa: col. 7 lines 44-46) and allowing the apparatus to have the program necessary for recovery in an area that has not been deactivated.

21. Okazawa further discloses, maintaining energy to only the control circuit (RAM 116) and the interface circuit (interface processor 111) during energy saving mode, while the remaining components are switched off (col. 7 lines 36-38).

22. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of JP 64-20185.

23. In accordance with claim 4, Okazawa discloses that programs for controlling the apparatus, thus including the interface control section, are stored in ROM 115.

24. Okazawa does not disclose expressly that when switching to energy saving mode, the program for controlling the interface circuit is transferred to image memory.

25. JP 64-20185 discloses that when transferring to energy saving mode, the CPU transfers a program stored in the ROM to the RAM (page 1 line 26 – page 2 line 3). Okazawa further discloses that during energy saving mode, only the interface processor 111 and the RAM 116 receive energy (col. 7 lines 36-38).

26. Okazawa and JP 64-20185 are combinable because they are from the same field of endeavor, namely energy saving image forming apparatuses.

27. Therefore, it would have been obvious to a person of ordinary skill in the art to transfer the control program for the interface section 150 of Okazawa's system from ROM 115 to RAM 116 as described by JP 64-20185, when entering energy saving mode.

28. The motivation for doing so would have been to operate only the RAM 116 and the interface processor 111 in the energy saving mode, thus reducing power consumption as compared with maintain power to other portions of the controller section (Okazawa: col. 7 lines 44-46) and allowing the apparatus to have the program necessary for recovery in an area that has not been deactivated.

29. Okazawa further discloses that the recovery of the system be initiated in response to an interrupt received by the interface section (col. 7 lines 4-6 and col. 8 lines 11-19).

Claim Rejections - 35 USC § 102

30. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated by Okazawa.

31. In accordance with claim 5, Okazawa discloses that when recovering to normal operating mode, part or all of the electronic parts that were operating in energy saving

states return to normal state upon execution of the recovery program; in Okazawa's system, when recovering to normal mode, the interface processor 111 activates power to the control section 110, which activates the remaining components in accordance with the flow chart of figure 3 (col. 8 lines 17-22).

32. Claim 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Okazawa.

33. In accordance with claim 6, Okazawa discloses an electronic printing apparatus 100-1 (figure 1), which receives and prints image data; in Okazawa's system, the controller section of the apparatus receives printing data and the engine section of the apparatus prints the image data (col. 4 lines 9-16).

34. Okazawa further discloses that the apparatus contains a print controller 110 (figure 1) for receiving image data (col. 4 lines 9-10) and controlling print sequence; in Okazawa's system, the controller section 110 has a program for controlling the entire apparatus (col. 4 lines 33-34).

35. Okazawa further discloses that the apparatus contains a print engine 120 (figure 1 and col. 4 lines 6-8). Okazawa further discloses that the printing engine prints images on a printing medium in accordance with a signal corresponding to the image data supplied by the print controller (col. 4 lines 58-61).

36. Okazawa further discloses that the print controller 110 (figure 1) contains a CPU 114 for executing required programs (col. 6 lines 57-60).

37. Okazawa further discloses an interface circuit 150 for receiving image data; in Okazawa's system the interface section 150 receives image data from hosts 130-1 or 130-2 (col. 4 lines 54-58).

38. Okazawa further discloses that the print controller is able to operate in a normal operating mode and an energy saving mode, which uses less energy than the normal mode; in Okazawa's system an interface processor 111 (figure 1) controls power to the controller and the engine, and is able to limit power supplied to the controller and the engine in a sleep state (col. 4 line 67 – col. 5 line 6). Okazawa further discloses that in energy saving mode, the interface circuit 111 is maintained in normal mode, while CPU 114 enters energy saving mode; in Okazawa's system, only the interface processor 111 and the RAM 116 are maintained in normal more while the remaining components are transferred to energy saving mode (col. 7 lines 36-38). Thus Okazawa meets all the limitations of claim 6.

Claim Rejections - 35 USC § 103

39. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of JP 64-20185.

40. In accordance with claim 7, discloses a CPU 114 that can operate in a normal mode and an energy saving mode (col. 4 line 67 – col. 5 line 6). Okazawa further discloses maintaining an interface circuit (interface processor 111) and a control circuit (RAM 116) in normal operating states, while the remainder of the components enter an energy saving mode (col. 7 lines 36-38). Okazawa does not disclose expressly that when switching from normal operating mode to energy saving mode the CPU is permitted to load a recovery program stored in program memory into an image memory.

41. JP 64-20185 discloses that when transferring to energy saving mode, the CPU transfers a program stored in the ROM to the RAM (page 1 line 26 – page 2 line 3).

42. Okazawa and JP 64-20185 are combinable because they are from the same field of endeavor, namely energy saving image forming apparatuses.

43. Therefore, it would have been obvious to a person of ordinary skill in the art to permit the CPU 114 of Okazawa's system to transfer a recovery program from the ROM 115 to the RAM 116 when entering energy saving mode, since in Okazawa's system the RAM 116 and the interface processor 111 are the only components which receive energy during energy saving mode (col. 7 lines 36-38).

44. The motivation for doing so would have been to operate only the RAM 116 and the interface processor 111 in the energy saving mode, thus reducing power consumption as compared with maintain power to other portions of the controller section (Okazawa: col. 7 lines 44-46) and allowing the apparatus to have the program necessary for recovery in an area that has not been deactivated.

Claim Rejections - 35 USC § 102

45. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Okazawa.

46. In accordance with claim 8, Okazawa discloses allowing the CPU 114 to return to a normal mode from an energy saving following the receipt of an interrupt originating at an interface circuit and a control circuit; in Okazawa's system, only the interface processor 111 (interface circuit) and RAM 116 (control circuit) are maintain in normal operating mode while the remaining components are in an energy saving mode (col. 7 lines 36-38), upon receipt of printing data, the interface processor 111 generates an interrupt (col. 7 lines 4-5), when an interrupt is received while the apparatus is in a sleep

mode (step 16 in figure 4), the interface processor 111 activates the controller section 110 which activates the remaining components (col. 8 lines 16-19).

47. Okazawa further discloses permitting the CPU to execute a recovery program; in Okazawa's system, when the interface processor 111 reactivates the control section 120, the CPU 114 executes the remaining recovery processes according to the flow chart of figure 3 (col. 8 lines 16-22 and col. 6 lines 57-61). Okazawa does not disclose expressly storing the program for the CPU in image memory, but the recovery program is stored in RAM as has been described above. It would be obvious to a person of ordinary skill in the art, that the recovered CPU could execute a program for recovering the remaining components from RAM, since the RAM is the only available memory area operating in normal operating mode.

48. Okazawa further discloses shifting all the electronic parts that are in the power saving mode to normal operating mode by execution of the recovery operation; in Okazawa's system the interface processor 111 and the RAM 116 remain in normal operating mode, while the remainder of the components enter the energy saving mode (col. 7 lines 36-38), when an interrupt is received, as described above, the interface processor 111 and the RAM 116 return the controller section 110 to normal operating mode (col. 17-19).

Claim Rejections - 35 USC § 103

49. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view of JP 64-20185.

50. In accordance with claim 9, discloses a CPU 114 that can operate in a normal mode and an energy saving mode (col. 4 line 67 – col. 5 line 6). Okazawa further discloses maintaining an interface circuit (interface processor 111) and a control circuit (RAM 116) in normal operating states, while the remainder of the components enter an energy saving mode (col. 7 lines 36-38). Okazawa does not disclose expressly that when switching from normal operating mode to energy saving mode the CPU is permitted to load a recovery program stored in program memory into an image memory.

51. JP 64-20185 discloses that when transferring to energy saving mode, the CPU transfers a program stored in the ROM to the RAM (page 1 line 26 – page 2 line 3).

52. Okazawa and JP 64-20185 are combinable because they are from the same field of endeavor, namely energy saving image forming apparatuses.

53. Therefore, it would have been obvious to a person of ordinary skill in the art to permit the CPU 114 of Okazawa's system to transfer a recovery program from the ROM 115 to the RAM 116 when entering energy saving mode, since in Okazawa's system the RAM 116 and the interface processor 111 are the only components which receive energy during energy saving mode (col. 7 lines 36-38).

54. The motivation for doing so would have been to operate only the RAM 116 and the interface processor 111 in the energy saving mode, thus reducing power consumption as compared with maintain power to other portions of the controller section (Okazawa: col. 7 lines 44-46) and allowing the apparatus to have the program necessary for recovery in an area that has not been deactivated.

55. Okazawa further discloses allowing the CPU 114 to return to a normal mode from an energy saving following the receipt of an interrupt originating at an interface circuit and a control circuit; in Okazawa's system, only the interface processor 111 (interface circuit) and RAM 116 (control circuit) are maintain in normal operating mode while the remaining components are in an energy saving mode (col. 7 lines 36-38), upon receipt of printing data, the interface processor 111 generates an interrupt (col. 7 lines 4-5), when an interrupt is received while the apparatus is in a sleep mode (step 16 in figure 4), the interface processor 111 activates the controller section 110 which activates the remaining components (col. 8 lines 16-19).

56. Okazawa further discloses permitting the CPU to execute a recovery program; in Okazawa's system, when the interface processor 111 reactivates the control section 120, the CPU 114 executes the remaining recovery processes according to the flow chart of figure 3 (col. 8 lines 16-22 and col. 6 lines 57-61). Okazawa does not disclose expressly storing the program for the CPU in image memory, but the recovery program is stored in RAM as has been described above. It would be obvious to a person of ordinary skill in the art, that the recovered CPU could execute a program for recovering the remaining components from RAM, since the RAM is the only available memory area operating in normal operating mode.

57. Okazawa further discloses shifting all the electronic parts that are in the power saving mode to normal operating mode by execution of the recovery operation; in Okazawa's system the interface processor 111 and the RAM 116 remain in normal operating mode, while the remainder of the components enter the energy saving mode

(col. 7 lines 36-38), when an interrupt is received, as described above, the interface processor 111 and the RAM 116 return the controller section 110 to normal operating mode (col. 17-19).

Contact Information

58. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karl R. Reitz whose telephone number is (703) 305-8696. The examiner can normally be reached on Monday-Friday 8:00-4:30.

59. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David K. Moore can be reached on (703) 305-7452. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

60. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9700.

KRR

DAVID MOORE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600